Researchers devise new method to arm electronic gadgets against power fluctuations

New Delhi, Jan 11th (India Science Wire): Indian researchers have developed the performance analysis of miniaturized circuitry used in modern devices such as mobile phones and tablets so that the devices may be designed for better performance even under erratic DC power supply.

“There is a need to understand the design equations that take into account the miniaturized parts of mixed electronic circuitry in order to improve the performance of the device and enhance the robustness of the components to power fluctuations”, says, Dr. Hitesh Shrimali, Associate Professor, School of Computing & Electrical Engineering, IIT Mandi. His research team analyses the losses that occur due to the power supply fluctuations to optimize the design specifications of mobile devices in terms of speed, power, gain, distortion levels, among others.

The electronic circuitry in modern devices including mobile phones, laptops and tablets comprises both analog and digital components on a single semiconductor IC. Such mixed signal circuits are powered by a direct current supply, often from an in-built battery. While these batteries have low voltages (3.7 V), the individual components of the miniaturized circuitry of mobile devices operate at even lower voltages. For example, transistors used in many modern circuitries are as small as 7 nanometres –100000 times smaller than the width of a single human hair and require voltages far below 1 V to work. Power spikes and fluctuations in the power source can degrade the performance of the mixed circuit over time. Thus, any fluctuations in the power of the battery can lead to significant performance deterioration. The designs of circuitry continue to use the concepts developed 20 years ago and have not considered the altered physics seen at nanometric size scales of modern electronics parts.

“Very Large-Scale Integration (VLSI) electronics are ubiquitous in today’s world, although we are not aware of it”, says Dr. Shrimali. Transceivers, antennae, amplifiers, Analog-to-Digital Converters (ADC), and Digital-to-Analog Converters (DAC) that are the heart of commonly used devices such as mobile phones, digital music players, laptops and tablets require such optimizations in design to extend their life and retain the quality of performance over time.

“We have used the matrix theory and closed-form of equations for transistors to analyse the key design specifications for the design of electronics that use VLSI of miniaturized components”, explain researchers. The published research will improve the efficiency of high speed on-chip systems, they added.

After developing the method, the team has verified the proof-of-concept using two examples of output stages for analog and digital blocks in a standard 180 nanometre technology with 1.8 V of supply and the same geometric area. Their models using the inspection method and the industry standard SPICE tools showed a maximum mean percentage error (MPE) of 3% for all the examples, which confirms the robustness of this approach in designing electronic components that are not adversely affected by power fluctuations.

This study, funded by the Ministry of Electronics and Information Technology (MeitY), has recently been published in IEEE Open Journal of Circuits and Systems. The research team consisted of Dr Hitesh Shrimali, IIT Mandi, research scholar Vijendra Kumar Sharma, IIT Mandi, and Dr Jai Narayan Tripathi from IIT Jodhpur. (India Science Wire)

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